ERLANGEN REGIONAL
COMPUTING CENTER

http://tiny.cc/NLPE-VSC

Node-Level Performance Engineering

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Three-day short course
Technische Universität Wien
Vienna Scientific Cluster
December 5-7, 2018

Course Schedule http://tiny.cc/NLPE-VSC

	Day 1
0900	Welcome & Intro
	Introduction to node-level computer architecture
	Tools: topology, affinity, clock speed
	Hands-On
	Microbenchmarking for architectural exploration
	Hands-On
	The Roofline performance model: basics
1700	End of day 1

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	Day 2
0900	Tools: hardware performance counters (+demo)
	Hands-On
	Programming for ccNUMA
	Single Instruction Multiple Data (SIMD) parallelism
	Simultaneous Multi-Threading (SMT)
	Case study: stencil algorithms
	Hands-On
1700	End of day 2

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	Day 3
0900	Case study: sparse matrix-vector multiplication (and friends)
	Hands-On
	Case study: tall & skinny matrix-matrix multiplication
	The Execution-Cache-Memory (ECM) performance model
	Hands-On
1630	End of day 3

Optionally we can use the afternoon of day 3 to cover special topics:

- Architecture and performance of the NEC SX-Aurora „Tsubasa“ vector processor
- Power and energy consumption aspects of computation