



References

**Selected papers on performance engineering
authored by the RRZE HPC group**

See also

<https://blogs.fau.de/hager/publications>



Book:

- G. Hager and G. Wellein: [Introduction to High Performance Computing for Scientists and Engineers](#). CRC Computational Science Series, 2010. ISBN 978-1439811924
<http://www.hpc.rrze.uni-erlangen.de/HPC4SE/>

Papers:

- J. Hofmann, D. Fey, M. Riedmann, J. Eitzinger, G. Hager, and G. Wellein: [Performance analysis of the Kahan-enhanced scalar product on current multi- and manycore processors](#). *Concurrency & Computation: Practice & Experience*. (2016). Available online, [DOI: 10.1002/cpe.3921](#).
Preprint: [arXiv:1604.01890](#)
- M. Röhrig-Zöllner, J. Thies, M. Kreuzer, A. Alvermann, A. Pieper, A. Basermann, G. Hager, G. Wellein, and H. Fehske: [Increasing the performance of the Jacobi-Davidson method by blocking](#). *SIAM Journal on Scientific Computing*, **37**(6), C697–C722 (2015). [DOI: 10.1137/140976017](#),
Preprint: <http://elib.dlr.de/89980/>
- T. M. Malas, G. Hager, H. Ltaief, H. Stengel, G. Wellein, and D. E. Keyes: [Multicore-optimized wavefront diamond blocking for optimizing stencil updates](#). *SIAM Journal on Scientific Computing* **37**(4), C439-C464 (2015). [DOI: 10.1137/140991133](#), Preprint: [arXiv:1410.3060](#)
- J. Hammer, G. Hager, J. Eitzinger, and G. Wellein: [Automatic Loop Kernel Analysis and Performance Modeling With Kerncraft](#). Proc. [PMBS15](#), the 6th International Workshop on Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems, in conjunction with ACM/IEEE Supercomputing 2015 ([SC15](#)), November 16, 2015, Austin, TX. [DOI: 10.1145/2832087.2832092](#),
Preprint: [arXiv:1509.03778](#)



Papers continued:

- M. Kreutzer, G. Hager, G. Wellein, A. Pieper, A. Alvermann, and H. Fehske: Performance Engineering of the Kernel Polynomial Method on Large-Scale CPU-GPU Systems. Proc. IPDPS15. DOI: [10.1109/IPDPS.2015.76](https://doi.org/10.1109/IPDPS.2015.76), Preprint: [arXiv:1410.5242](https://arxiv.org/abs/1410.5242)
- M. Wittmann, G. Hager, T. Zeiser, J. Treibig, and G. Wellein: Chip-level and multi-node analysis of energy-optimized lattice-Boltzmann CFD simulations. Concurrency and Computation: Practice and Experience (2015). DOI: [10.1002/cpe.3489](https://doi.org/10.1002/cpe.3489) Preprint: [arXiv:1304.7664](https://arxiv.org/abs/1304.7664)
- H. Stengel, J. Treibig, G. Hager, and G. Wellein: Quantifying performance bottlenecks of stencil computations using the Execution-Cache-Memory model. Proc. ICS15, DOI: [10.1145/2751205.2751240](https://doi.org/10.1145/2751205.2751240), Preprint: [arXiv:1410.5010](https://arxiv.org/abs/1410.5010)
- M. Kreutzer, G. Hager, G. Wellein, H. Fehske, and A. R. Bishop: A unified sparse matrix data format for modern processors with wide SIMD units. SIAM Journal on Scientific Computing **36**(5), C401–C423 (2014). DOI: [10.1137/130930352](https://doi.org/10.1137/130930352), Preprint: [arXiv:1307.6209](https://arxiv.org/abs/1307.6209)
- G. Hager, J. Treibig, J. Habich and G. Wellein: Exploring performance and power properties of modern multicore chips via simple machine models. Computation and Concurrency: Practice and Experience (2013). DOI: [10.1002/cpe.3180](https://doi.org/10.1002/cpe.3180), Preprint: [arXiv:1208.2908](https://arxiv.org/abs/1208.2908)
- J. Treibig, G. Hager and G. Wellein: Performance patterns and hardware metrics on modern multicore processors: Best practices for performance engineering. Workshop on Productivity and Performance (PROPER 2012) at Euro-Par 2012, August 28, 2012, Rhodes Island, Greece. DOI: [10.1007/978-3-642-36949-0_50](https://doi.org/10.1007/978-3-642-36949-0_50). Preprint: [arXiv:1206.3738](https://arxiv.org/abs/1206.3738)



Papers continued:

- M. Wittmann, T. Zeiser, G. Hager, and G. Wellein: **Comparison of Different Propagation Steps for Lattice Boltzmann Methods**. Computers & Mathematics with Applications (Proc. ICMMS 2011). Available online, [DOI: 10.1016/j.camwa.2012.05.002](https://doi.org/10.1016/j.camwa.2012.05.002). Preprint:[arXiv:1111.0922](https://arxiv.org/abs/1111.0922)
- M. Kreutzer, G. Hager, G. Wellein, H. Fehske, A. Basermann and A. R. Bishop: **Sparse Matrix-vector Multiplication on GPGPU Clusters: A New Storage Format and a Scalable Implementation**. Workshop on Large-Scale Parallel Processing 2012 (LSPP12), [DOI: 10.1109/IPDPSW.2012.211](https://doi.org/10.1109/IPDPSW.2012.211)
- J. Treibig, G. Hager, H. Hofmann, J. Hornegger and G. Wellein: **Pushing the limits for medical image reconstruction on recent standard multicore processors**. International Journal of High Performance Computing Applications, (published online before print). [DOI: 10.1177/1094342012442424](https://doi.org/10.1177/1094342012442424)
- G. Wellein, G. Hager, T. Zeiser, M. Wittmann and H. Fehske: **Efficient temporal blocking for stencil computations by multicore-aware wavefront parallelization**. Proc. COMPSAC 2009. [DOI: 10.1109/COMPSAC.2009.82](https://doi.org/10.1109/COMPSAC.2009.82)
- M. Wittmann, G. Hager, J. Treibig and G. Wellein: **Leveraging shared caches for parallel temporal blocking of stencil codes on multicore processors and clusters**. Parallel Processing Letters **20** (4), 359-376 (2010). [DOI: 10.1142/S0129626410000296](https://doi.org/10.1142/S0129626410000296). Preprint: [arXiv:1006.3148](https://arxiv.org/abs/1006.3148)
- J. Treibig, G. Hager and G. Wellein: **LIKWID: A lightweight performance-oriented tool suite for x86 multicore environments**. Proc. [PSTI2010](https://doi.org/10.1109/ICPPW.2010.38), the First International Workshop on Parallel Software Tools and Tool Infrastructures, San Diego CA, September 13, 2010. [DOI: 10.1109/ICPPW.2010.38](https://doi.org/10.1109/ICPPW.2010.38). Preprint: [arXiv:1004.4431](https://arxiv.org/abs/1004.4431)



Papers continued:

- G. Schubert, H. Fehske, G. Hager, and G. Wellein: **Hybrid-parallel sparse matrix-vector multiplication with explicit communication overlap on current multicore-based systems**. *Parallel Processing Letters* 21(3), 339-358 (2011).
[DOI: 10.1142/S0129626411000254](https://doi.org/10.1142/S0129626411000254)
- J. Treibig, G. Wellein and G. Hager: **Efficient multicore-aware parallelization strategies for iterative stencil computations**. *Journal of Computational Science* 2 (2), 130-137 (2011). [DOI: 10.1016/j.jocs.2011.01.010](https://doi.org/10.1016/j.jocs.2011.01.010)
- K. Iglberger, G. Hager, J. Treibig, and U. Rde: **Expression Templates Revisited: A Performance Analysis of Current ET Methodologies**. *SIAM Journal on Scientific Computing* 34(2), C42-C69 (2012). [DOI: 10.1137/110830125](https://doi.org/10.1137/110830125), Preprint: [arXiv:1104.1729](https://arxiv.org/abs/1104.1729)
- K. Iglberger, G. Hager, J. Treibig, and U. Rde: **High Performance Smart Expression Template Math Libraries**. 2nd International Workshop on New Algorithms and Programming Models for the Manycore Era ([APMM 2012](#)) at [HPCS 2012](#), July 2-6, 2012, Madrid, Spain. [DOI: 10.1109/HPCSim.2012.6266939](https://doi.org/10.1109/HPCSim.2012.6266939)
- J. Habich, T. Zeiser, G. Hager and G. Wellein: **Performance analysis and optimization strategies for a D3Q19 Lattice Boltzmann Kernel on nVIDIA GPUs using CUDA**. *Advances in Engineering Software and Computers & Structures* 42 (5), 266–272 (2011). [DOI: 10.1016/j.advengsoft.2010.10.007](https://doi.org/10.1016/j.advengsoft.2010.10.007)
- J. Treibig, G. Hager and G. Wellein: **Multicore architectures: Complexities of performance prediction for Bandwidth-Limited Loop Kernels on Multi-Core Architectures**.
[DOI: 10.1007/978-3-642-13872-0_1](https://doi.org/10.1007/978-3-642-13872-0_1), Preprint: [arXiv:0910.4865](https://arxiv.org/abs/0910.4865).



Papers continued:

- G. Hager, G. Jost, and R. Rabenseifner: **Communication Characteristics and Hybrid MPI/OpenMP Parallel Programming on Clusters of Multi-core SMP Nodes**. In: Proceedings of the Cray Users Group Conference 2009 (CUG 2009), Atlanta, GA, USA, May 4-7, 2009. [PDF](#)
- R. Rabenseifner and G. Wellein: **Communication and Optimization Aspects of Parallel Programming Models on Hybrid Architectures**. International Journal of High Performance Computing Applications **17**, 49-62, February 2003.
[DOI:10.1177/1094342003017001005](https://doi.org/10.1177/1094342003017001005)